PLL 的使用

1. PLL 作用：用于生成我们设计所需要的时钟频率

- 将输入的时钟进行倍频和分频，并且其相位偏移、占空比等和等都可以控制。
- 倍频只能通过 PLL 来实现。
- 当 FPGA 有 PLL 时，建议用 PLL 生成所需要的时钟频率。不建议通过计数器分频等来实现。

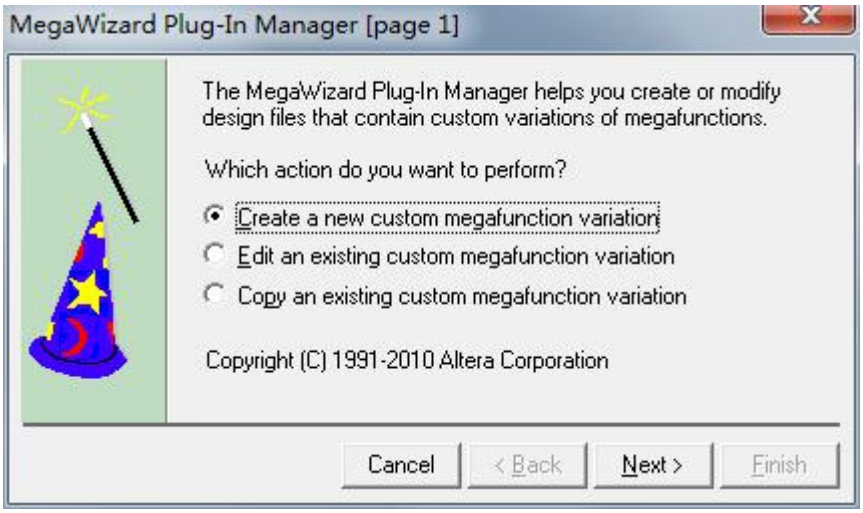
2.要求：无需深究其运行机理，主要会用，在 quartusII 里面可以直接生成

使用过程

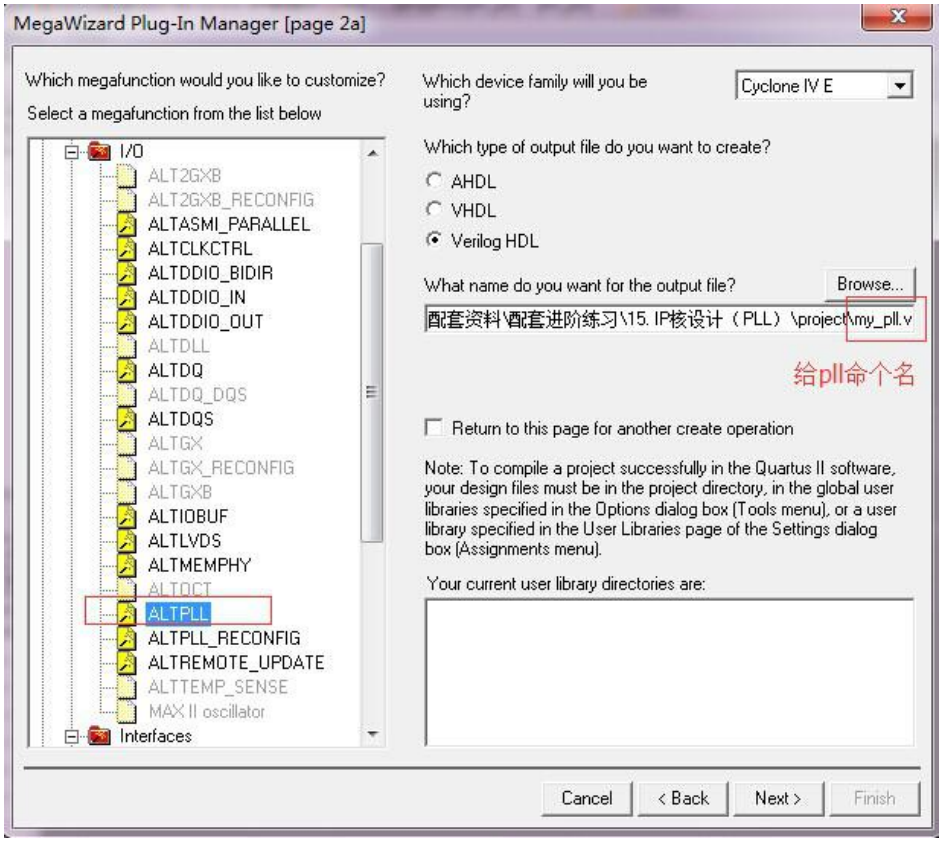
1. 打开 IP 核管理工具

a 打开 quartus 软件

b Tools -> MegaWizard，弹出如下界面

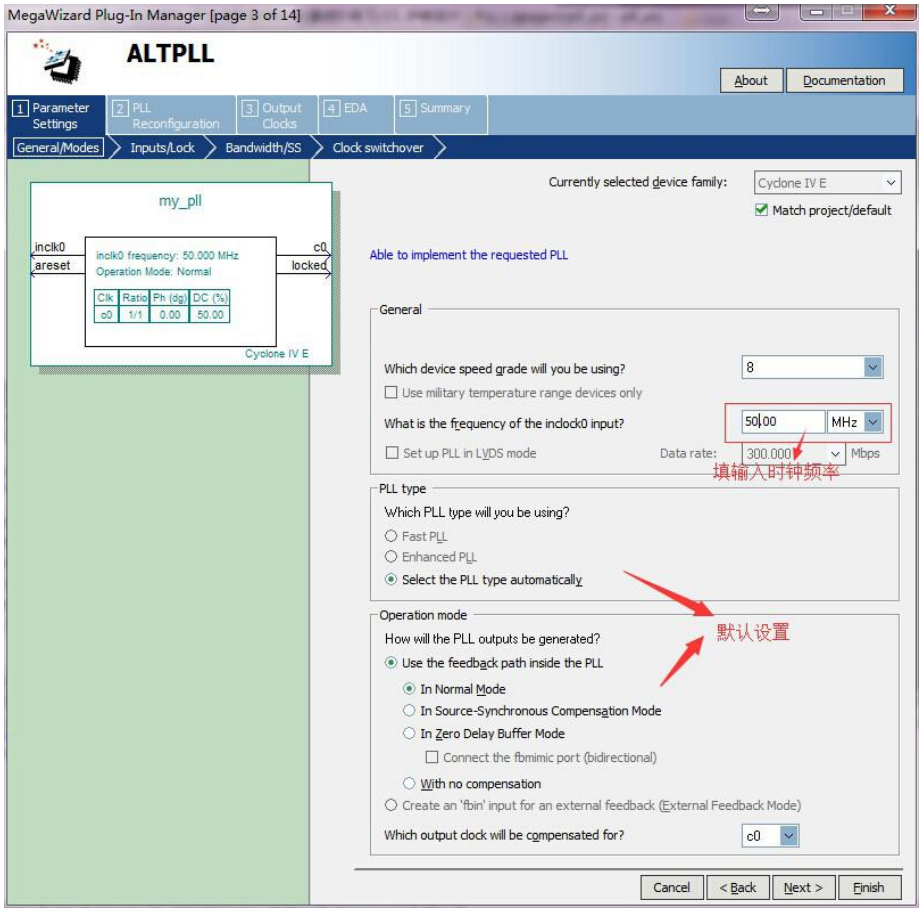


c 默认选择生成新的 IP 文件，选 next。弹出如下窗口。

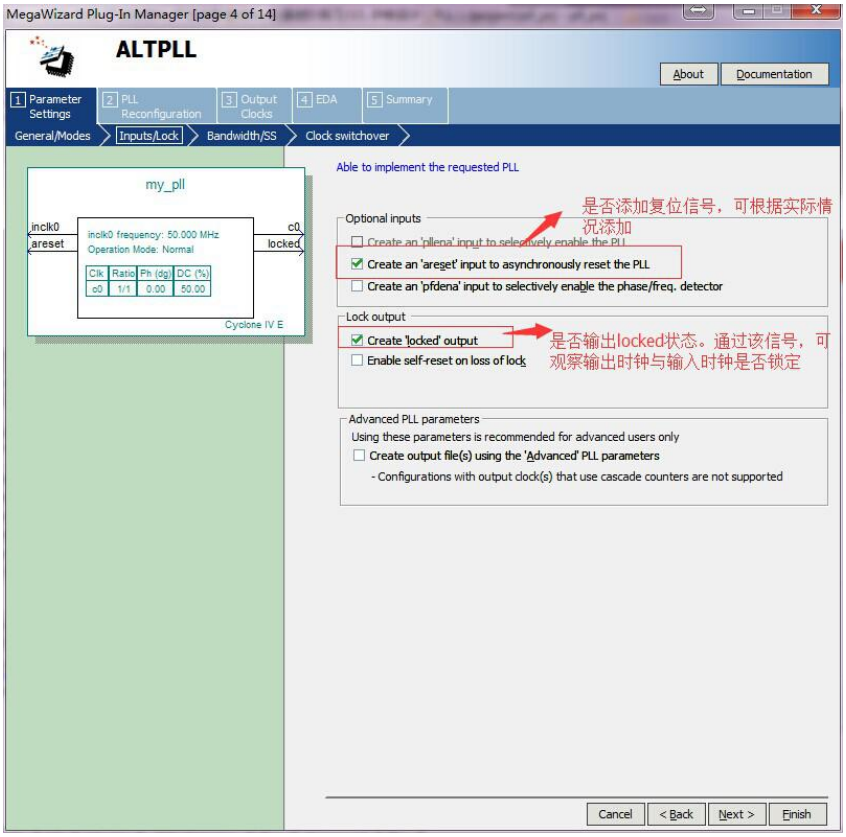


d　按图上选择 ALTPLL，并且在右边起个文件名。然后点 Next 就可以开始设置参数了。

2.设置 IP 参数

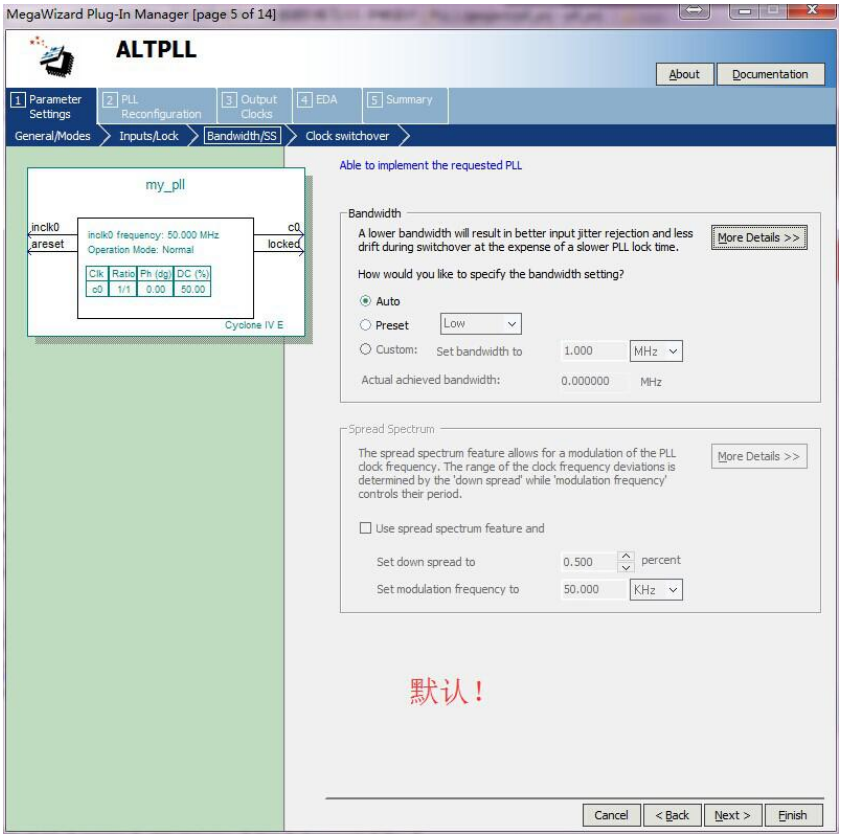


上图中，主要是设置输入的时钟频率，例如明德扬开发板输入时钟是固定的 50MHz，因此此时可填写 50。其他默认，按 next。



上图 1 中，关注是否要有复位信号。如果项目需要复位，则勾选，不需要则不勾选。

上图 2 中，问是否要有 locked 指示信号。该信号为 1，表示时钟输出稳定可用。可根据需要勾选。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Inputs/Lock
Bandwidth/SS
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my_pll
inclk0
areset
c0
locked
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 1/1 0.00 50.00
Cyclone IV E
Able to implement the requested PLL
Bandwidth
A lower bandwidth will result in better input jitter rejection and less drift during switchover at the expense of a slower PLL lock time.
More Details >>
How would you like to specify the bandwidth setting?
Auto
Preset
Low
Custom:
Set bandwidth to
1.000
MHz
Actual achieved bandwidth:
0.000000
MHz
Spread Spectrum
The spread spectrum feature allows for a modulation of the PLL clock frequency. The range of the clock frequency deviations is determined by the 'down spread' while 'modulation frequency' controls their period.
More Details >>
Use spread spectrum feature and
Set down spread to
0.500
percent
Set modulation frequency to
50.000
KHz
默认！
Cancel
< Back
Next >
Finish


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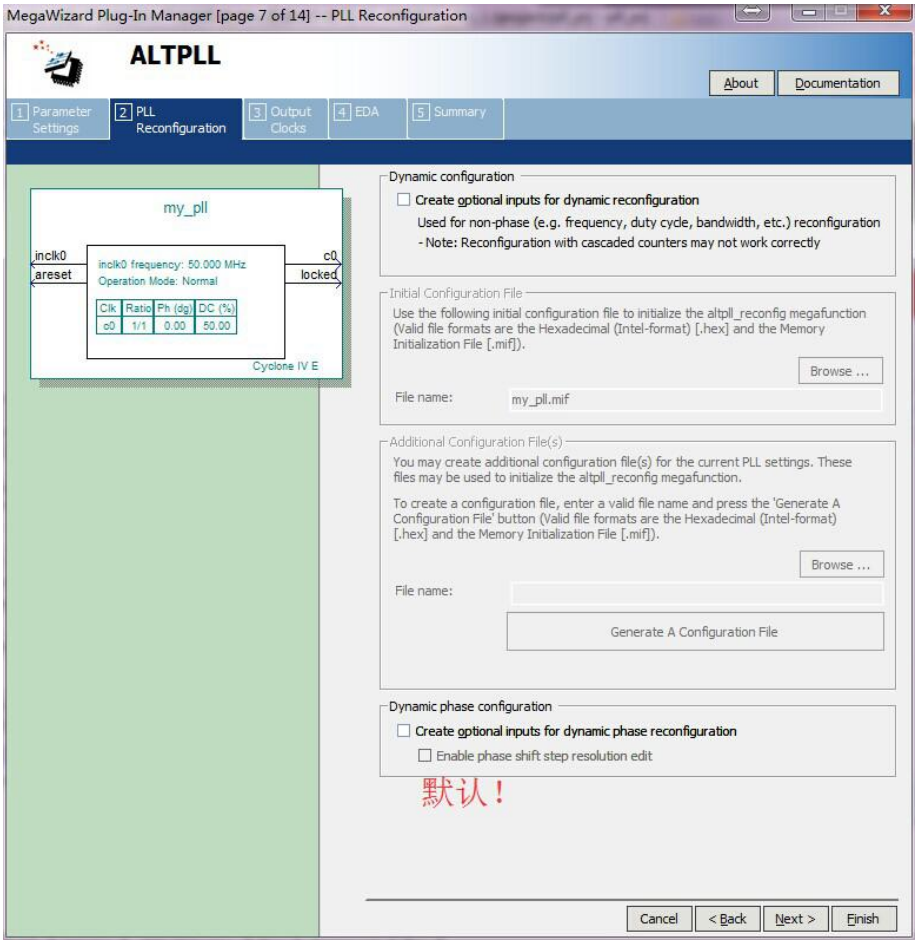
inclk0
areset
c0
locked
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 1/1 0.00 50.00
Cyclone IV E
Able to implement the requested PLL
Clock switchover
Create an 'inclk1' input for a second input clock
What is the frequency of the inclock1 input?
100.00
MHz
Input clock switch
Create a 'clkswitch' input to manually select between the input clocks
(The clkswitch input will behave as an input clock selection control input)
Allow PLL to automatically control the switching between input clocks
(The clkswitch input will behave as a manual override control input)
Create a 'clkswitch' input to dynamically toggle between input clocks
Perform the input clock switchover after
1
input clock cycles
Create an 'activeclock' output to indicate the input clock being used
(0 inclk0 is being used/ 1 inclk1 is being used)
Create a 'clkbad' output for each input clock
(0 input clock is toggling/ 1 input clock is not toggling)
增加输入时钟。由于我们只有一个输入时钟，所以只用inclk0即可，无需增加。
Cancel
< Back
Next >
Finish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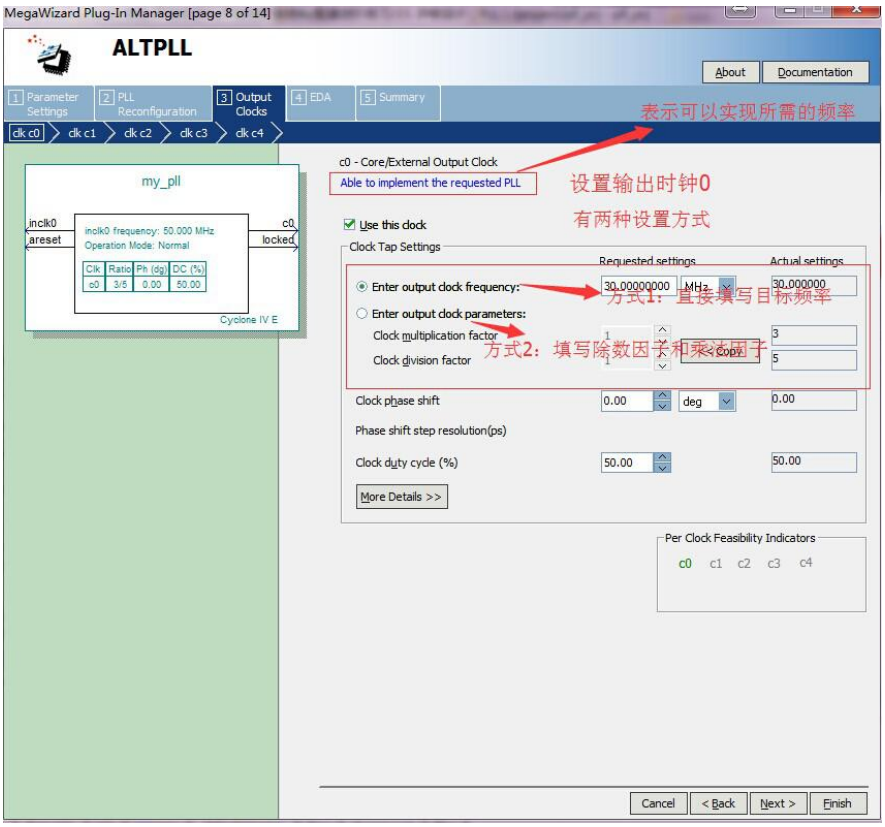
my_pll
inclk0
areset
c0
locked
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk | Ratio | Ph (dg) | DC (%)
c0 | 1/1 | 0.00 | 50.00
Cyclone IV E
Dynamic configuration
Create optional inputs for dynamic reconfiguration
Used for non-phase (e.g. frequency, duty cycle, bandwidth, etc.) reconfiguration
- Note: Reconfiguration with cascaded counters may not work correctly
Initial Configuration File
Use the following initial configuration file to initialize the altpll_reconfig megafunction (Valid file formats are the Hexadecimal (Intel-format) [.hex] and the Memory Initialization File [.mif]).
Browse ...
File name:
my_pll.mif
Additional Configuration File(s)
You may create additional configuration file(s) for the current PLL settings. These files may be used to initialize the altpll_reconfig megafunction.
To create a configuration file, enter a valid file name and press the 'Generate A Configuration File' button (Valid file formats are the Hexadecimal (Intel-format) [.hex] and the Memory Initialization File [.mif]).
Browse ...
File name:
Generate A Configuration File
Dynamic phase configuration
Create optional inputs for dynamic phase reconfiguration
Enable phase shift step resolution edit
默认！
Cancel
< Back
Next >
Finish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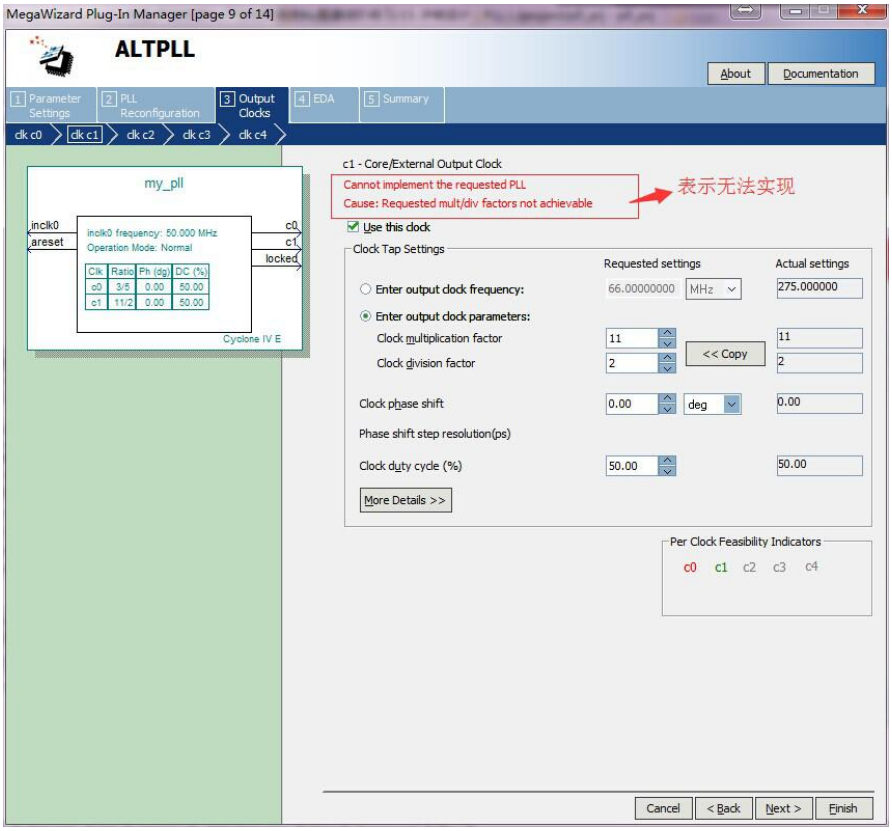
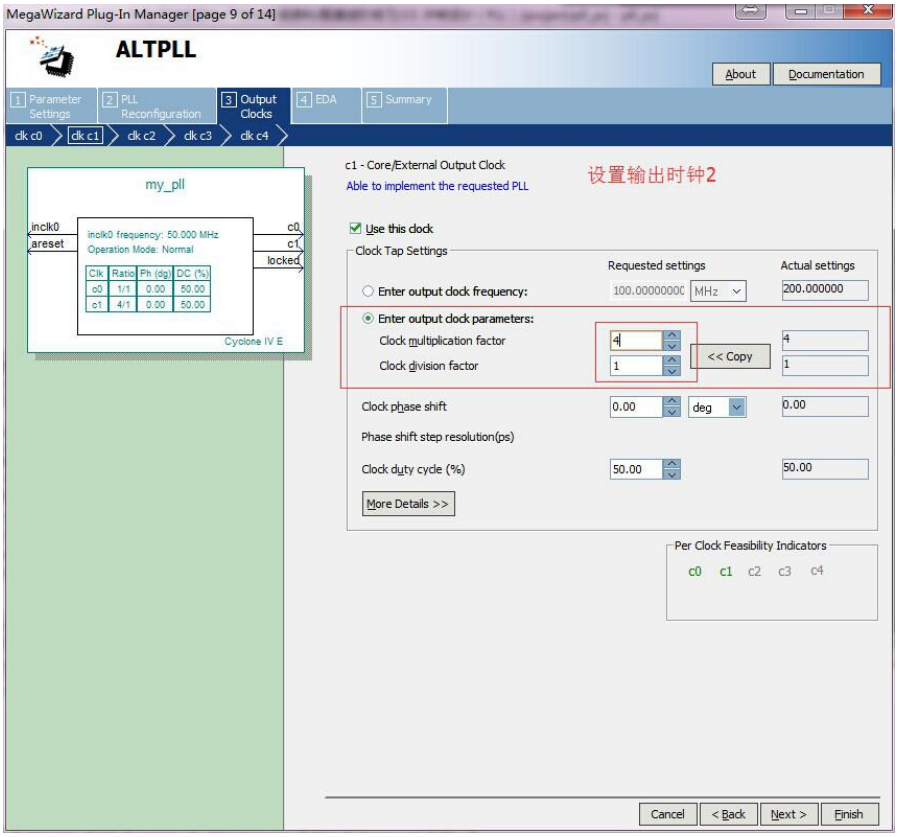
clk c0
clk c1
clk c2
clk c3
clk c4
表示可以实现所需的频率
my_pll
inclk0
areset
c0
locked
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk | Ratio | Ph (dg) | DC (%)
c0 | 3/5 | 0.00 | 50.00
Cyclone IV E
c0 - Core/External Output Clock
Able to implement the requested PLL
设置输出时钟0
有两种设置方式
Use this clock
Clock Tap Settings
Requested settings
Actual settings
Enter output clock frequency:
30.00000000
MHz
30.000000
方式1：直接填写目标频率
Enter output clock parameters:
Clock multiplication factor
Clock division factor
3
5
方式2：填写除数因子和乘法因子
Clock phase shift
0.00
deg
0.00
Phase shift step resolution(ps)
Clock duty cycle (%)
50.00
50.00
More Details >>
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish

设置 c0 的输出频率。PLL 的每个频率都有一个预 scale 系数（N）和一个乘法系数（M），范围从 1 到 32。其输出公式为：

输出时钟频率 = 输入时钟频率*（M/N）

输出的时钟频率只能由上述公式产生，如果产生不了，则会提示报错。如下图。

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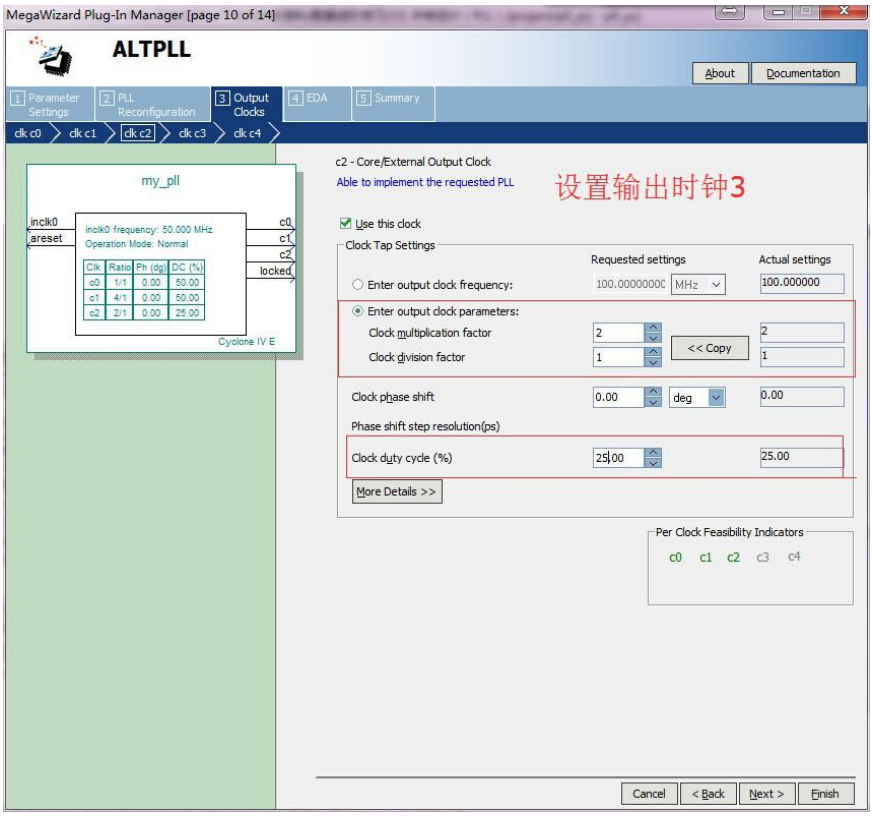
5 Summary
clk c0
clk c1
clk c2
clk c3
clk c4
my_pll
inclk0
areset
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 1/1 0.00 50.00
c1 4/1 0.00 50.00
c0
c1
locked
Cyclone IV E
c1 - Core/External Output Clock
Able to implement the requested PLL
设置输出时钟2
Use this clock
Clock Tap Settings
Requested settings
Actual settings
Enter output clock frequency:
100.00000000 MHz
200.000000
Enter output clock parameters:
Clock multiplication factor
4
4
Clock division factor
1
<< Copy
1
Clock phase shift
0.00
deg
0.00
Phase shift step resolution(ps)
Clock duty cycle (%)
50.00
50.00
More Details >>
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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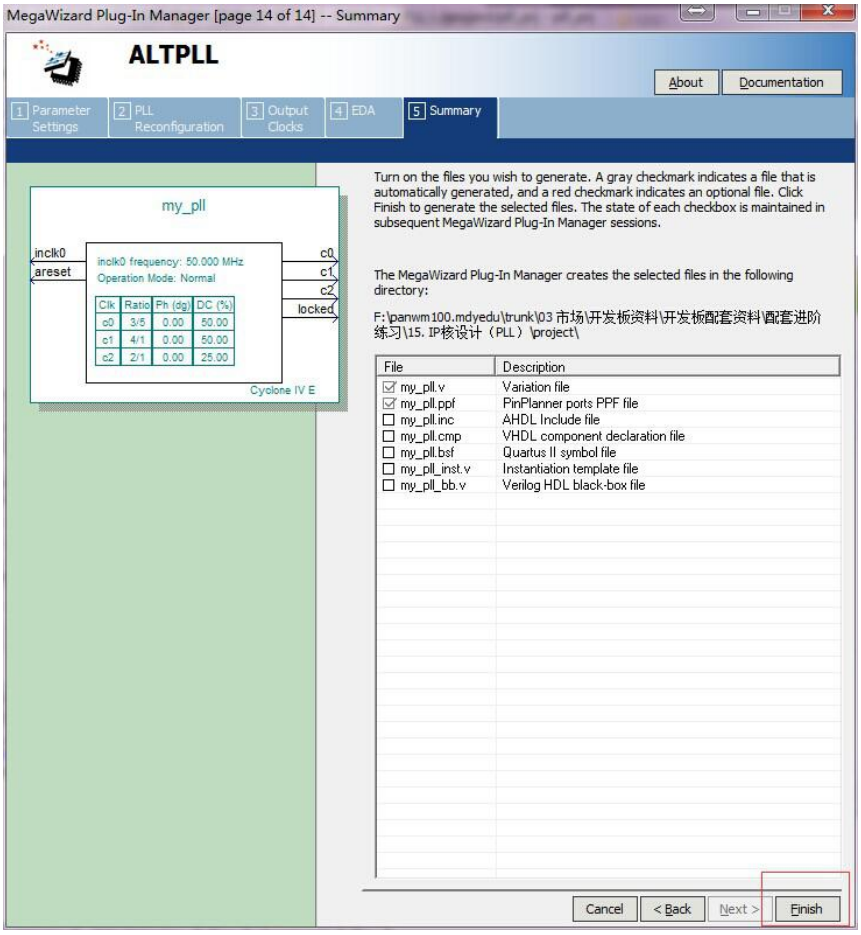
clk c0
clk c1
clk c2
clk c3
clk c4
my_pll
inclk0
areset
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 1/1 0.00 50.00
c1 4/1 0.00 50.00
c2 2/1 0.00 25.00
c0
c1
c2
locked
Cyclone IV E
c2 - Core/External Output Clock
Able to implement the requested PLL
设置输出时钟3
Use this clock
Clock Tap Settings
Requested settings
Actual settings
Enter output clock frequency:
100.00000000 MHz
100.000000
Enter output clock parameters:
Clock multiplication factor
2
2
Clock division factor
1
<< Copy
1
Clock phase shift
0.00
deg
0.00
Phase shift step resolution(ps)
Clock duty cycle (%)
25.00
25.00
More Details >>
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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5 Summary
my_pll
inclk0
areset
inclk0 frequency: 50.000 MHz
Operation Mode: Normal
Clk | Ratio | Ph (dg) | DC (%)
c0 | 3/5 | 0.00 | 50.00
c1 | 4/1 | 0.00 | 50.00
c2 | 2/1 | 0.00 | 25.00
c0
c1
c2
locked
Cyclone IV E
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a red checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
F:\panwm100.mdyedu\trunk\03 市场\开发板资料\开发板配套资料\配套进阶练习\15. IP核设计（PLL）\project\
File
Description
my_pll.v
Variation file
my_pll.ppf
PinPlanner ports PPF file
my_pll.inc
AHDL Include file
my_pll.cmp
VHDL component declaration file
my_pll.bsf
Quartus II symbol file
my_pll_inst.v
Instantiation template file
my_pll_bb.v
Verilog HDL black-box file
Cancel
< Back
Next >
Finish