

明德扬科技教育有限公司

生成 FIFO 的 IP 核

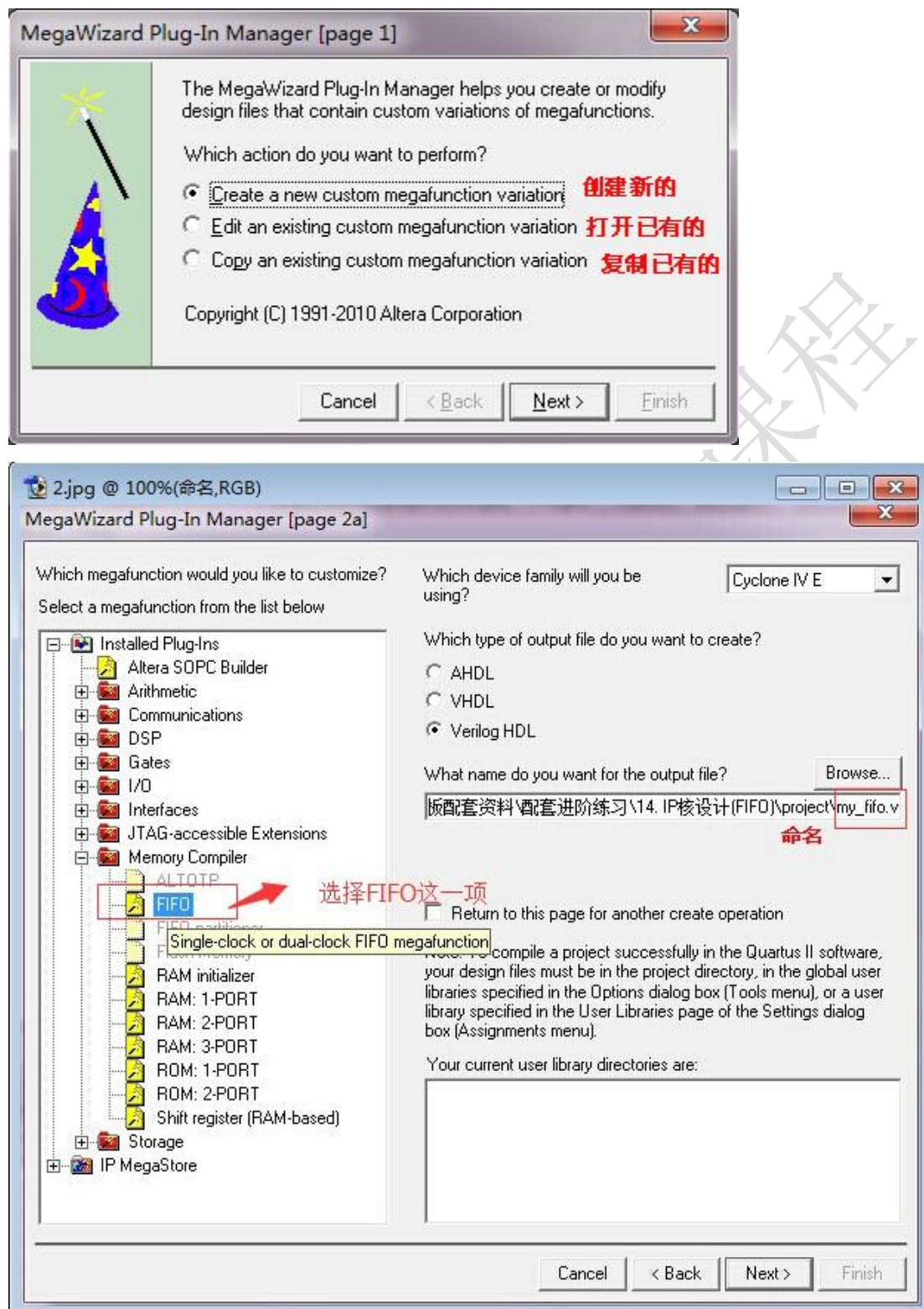
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打开 quartus 软件，然后 TOOL，选择 MegaWizard 选项，弹出如下图：



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FIFO

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Documentation

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2 EDA
3 Summary

Width, Clks, Synchronization
DCFIFO 1
DCFIFO 2
Rdreq Option, Blk Type
Optimization, Circuitry Protection

my_fifo

data[15..0]

wrreq

wrclk

rdreq (aok)

rdclk

wrfull

wrempty

wrusedw[5..0]

q[15..0]

rdfull

rdempty

rdusedw[5..0]

16 bits x 64 words

Currently selected device family: Cydome IV E

☒ Match project/default

How wide should the FIFO be? 16 bits

☐ Use a different output width and set to 16 bits

How deep should the FIFO be? 64 words

Do you want a common clock for reading and writing the FIFO?

☐ Yes, synchronize both reading and writing to 'dclk'.
Create one set of full/empty control signals.

☒ No, synchronize reading and writing to 'rdclk' and 'wrclk', respectively. Create a set of full/empty control signals for each clock.

Resource Usage

20 lut + 1 M9K + 90 reg

Cancel
< Back
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Finish

如果读和写时钟相同，选此项

如果读和写时钟不同，选此项

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my_fifo

Latency and Related Options

Total latency, clock synchronization, metastability protection, area, and fmax options must be set as a group. Total latency is the sum of two write clock rising edges and the number of read clocks selected below.

Which option(s) is most important to the DCFIFO?
(Read clk sync stages, metastability protection, area, fmax)

☒ **Lowest latency but requires synchronized clocks**
 1 sync stage, no metastability protection, smallest size, good fmax

☐ **Minimal setting for unsynchronized clocks**
 2 sync stages, good metastability protection, medium size, good fmax

☐ **Best metastability protection, best fmax, unsynchronized clocks**
 3 or more sync stages, best metastability protection, largest size, best fmax

How many sync stages? 3

优化选项

Resource Usage

20 lut + 1 M9K + 90 reg

Cancel

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my_fifo

16 bits x 64 words

Which optional output control signals do you want?

Read-side

☒ full

☒ empty

☒ usedw[]

Note: These signals are synchronous to 'rdclk'

Write-side

☒ full

☒ empty

☒ usedw[]

Note: These signals are synchronous to 'wrclk'

FIFO的指示信号，有部分会用到

usedw[] is the number of words in the FIFO. Note: You can use the MSB to generate a half-full flag.

☐ Add an extra MSB to usedw port(s)

☐ Asynchronous clear

Note: For more accurate timing analysis, use the TimeQuest Timing Analyzer. If you are using the Classic Timing Analyzer, turn on the Enable Recovery/Removal analysis option.

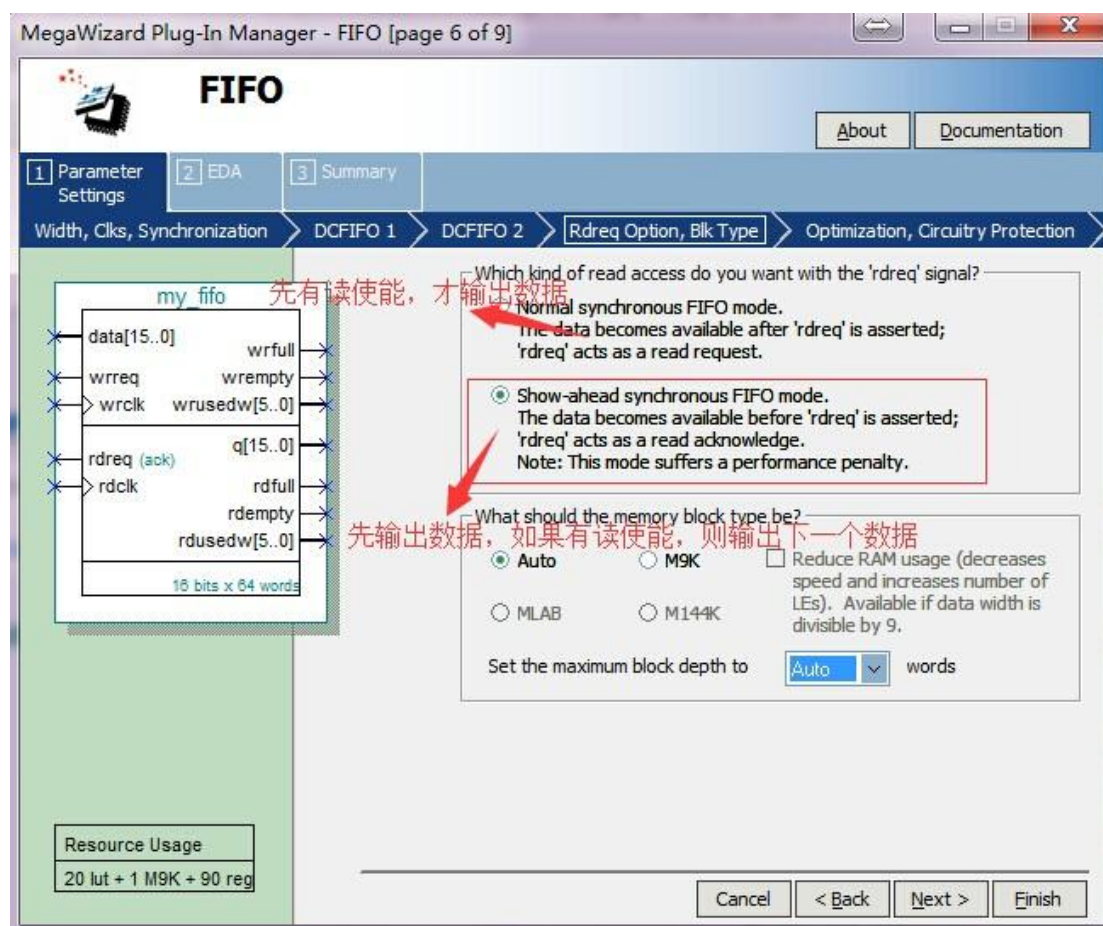
☐ Add circuit to synchronize 'aclr' input with 'wrclk'

Resource Usage

20 lut + 1 M9K + 90 reg

Cancel < Back Next > Finish

注意：一般勾选 read-side 的 empty, write-side 的 full。因为通常读时，要判断是否空了；写时，要判断是否满了。



重点：Show-ahead 是先输出数据，如果有读使能，再输出下一个数据。我经常使用这种模式，亦推荐大家使用。

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data[15..0]

wrreq

wrclk

rdreq (ack)

rdclk

wrusedw[5..0]

q[15..0]

rdusedw[5..0]

16 bits x 64 words

Would you like to disable any circuitry protection?
If not required, overflow and underflow checking can be disabled to improve performance.

☐ Disable overflow checking. Writing to a full FIFO will corrupt contents.

☐ Disable underflow checking. Reading from an empty FIFO will corrupt contents.

☐ Implement FIFO storage with logic cells only, even if the device contains memory blocks

Resource Usage

16 lut + 1 M9K + 100 reg

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Resource Usage

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my_fifo

16 bits x 64 words

Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a red checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:

F:\panwm100.mdyedu\trunk\03 市场\开发板资料\开发板配套资料\配套进阶练习\14. IP核设计(FIFO)\project\

File	Description
<input checked="" type="checkbox"/> my_fifo.v	Variation file
<input type="checkbox"/> my_fifo.inc	AHDL Include file
<input type="checkbox"/> my_fifo.cmp	VHDL component declaration file
<input type="checkbox"/> my_fifo.bsf	Quartus II symbol file
<input type="checkbox"/> my_fifo_inst.v	Instantiation template file
<input type="checkbox"/> my_fifo_bb.v	Verilog HDL black-box file
<input type="checkbox"/> my_fifo_waveforms.html	
<input type="checkbox"/> my_fifo_wave*.jpg	

Resource Usage
20 lut + 1 M9K + 90 reg

Cancel < Back Next > Finish